DIGITAL EDUCATION
MARTCOST

COMPUTER SCIENCE & ENGINEERING

INFORMATION TECHNOLOGY

Computer Organization

Hand Notes For GATE, PSUs & Competitive Exam

Hand Notes

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Computer Organization

1. Number System & Representation

2. Memory Organization : Hierarchy
   Cache Memory – Address mapping
   – Updation
   – Replacement
   Principles of virtual memory & Associate memory

3. Fixed Point Arithmetic, Carry look ahead ac

4. Instructions, Addressing Modes, Instructio pipeline, control unit design

5. Addressing, Data Transfer Techniq
   Disk & tape memories

1, 3, 4 : Computer Architecture – J. P. Hayes
2, 5 : Computer organization – Pauls choudhar

CA: It deals with conceptual view things of the system
- Instruct^n set
- Addressing Modes
- Data format

Instruct^n Set
- CISC (Intel)
- RISC (Risk) (Reduced Inst. set) (PowerPC) "fixed length"

(Not advantage) Supports limited Addressing mode //
// If any instr. will not complete at at CPI = 1 (clock per instr.), then it is not a part of RISC
// No more registers are required.
// Ctd provides only flexibility

// Instr. have - | OPcode | Ref. opr |
Reference of operand.
by Ref opr part, we can easily get the instr. addr.
// Data format deals with 'How to interpret the binary string'

23/09/10

Instruction Pipelining

Register,

→ Efficient usage of resources. (Instruction phase are overlapped)

→ Performance of pipelining is given by speedup factor, S = time without pipeline / time with pipeline

se address gister

→ Ideal case with k-stage instruct^n pipeline

$$T_n = (K+n-1)\,t_p \quad T_{clock} = t_p, \quad S_{ideal} = K, \quad CPI_{avg} = 1$$

is ed in it ing.

→ Parameters influencing the performance
- Un-even stage delays
- Buffer overhead
- Dependencies among the instruct^n

→ Data dependencies occurs when the result of one instruct^n is to be used by its successor.

→ Instruct^n re-scheduling stall cycles introduct & [operand forwarding] techniques deal with data dependencies.

→ Control dependencies occur when flow of execu is altered by instruct^n cycles of another. [Branch instructns] are the main resources for control dependencies.

→ Delayed-Branch, Multiple pipes & [prediction] are used to deal control dependencies

(1) If processor register will be of operand

(1) Index - Then it is Index Register.

⇒ used for accessing the arrays.

(2) Base address of operand - Base address Register

⇒ used for relocatable prog's.

⇒ Prob occurs with JUMP instr.

Used for in

(3) Relative Addressing - PC is involved in it

Used for intrasegment branching.

(4) Based Index Relative

A(0,0)
A(1,0)
A(2,0)
A(3,0)

(0,0)
(1,0)
(0,1)
(1,1)

Principle of Associate Memory

"The associate memory is also called a content addressable memory. To retrieve the info., the content or partial conten is used, since no address is involved, it is the fastest memory."

The associate memory contains:

(1) argument Register (n)
(2) Key Register (mask register (mask)) (n)
(3) Associate memory array (mxn)
(4) Match logic (mx1)

→ To perform the read oprn, place that cont or partial content in the argument regist The match logic will generate either sing or multiple match word.

→ In case of multiple matching, the matched words are accessed sequentially until the desired word is obtained.

→ To perform the write oprn, place the wo in argument register, if it is not already existing then it is to be moved into one of the free locatn.

→ The match logic expression for ith word, (Complete Matching) $M_i = \prod_{j=0}^{n-1} (F_j \odot A_j)$

A(0,0) — M ← R Column-Major Order

H ← W

A(0,1) — M ← R

H ← W

Hits : 100

A(0,0)
A(0,1)
A(0,2) occupies

400 words

Block 0

A(0,0)
A(1,0)
A(2,0)
A(3,0)
A(8,0)
A(9,0)
A(0,1)
A(1,1)

If the array is arranged in Column major order for every element, a block is moved from main memory to cache, total blocks moved are 100. For every block two references are made, one of them result Hit. No. of Hit = 100

Hit ratio = 0.5 (50%)